IN THE DRAWINGS

FIGS. 1-4 have been designated as PRIOR ART. Further, FIGS. 4 and 11 have had a typographic correction made to change the word 'initialiging' to 'initializing,' and 'initialige' to 'initialize.'

REMARKS

Claims 1-21 are pending in the application.

The specification was objected to by the Examiner for the user of the term 'discloses' in the Abstract. This has been corrected by amendments to the specification above. Withdrawal of this objection is therefore requested.

The drawings filed on 08 April 2004 were objected to by the Examiner, as FIGs. 1-4 should be designated as prior art. A proposed drawing amendment is including with this response. Formal drawings in accordance with these amendments will be sent when the drawing correction is approved. Approval of the proposed amendment is requested.

The drawings and/or the specification were objected to because of the use of reference figures in the drawings that were not in the specification. Amendments to the specification above have corrected this situation. Withdrawal of this objection is therefore requested.

Claims 1-3, 5, 7-9, 11, 13-15 and 17 are rejected under 35 U.S.C. 103(a) over the Applicant Admitted Prior Art (AAPA) in view of U.S. Patent No. 4,654,695, to Fling.

The office action states that the AAPA teaches 'a memory system having a plurality of memory chips comprising a memory cell array (60)...". However, the memory cell array 60 of Figure 2 is for a single-chip. The discussion in the Background of the Invention with regard to Figures 1-4 is all directed to single-chip implementations. See the specification, page 1, lines 28-29, "...FIG. 1...as an example in a single chip..." page 2, lines 3-4, "FIG. 2...in a single chip..." page 2, lines 11-12, "FIGs. 3 and 4...in a single chip..." Nowhere in the Background of the Invention or the related drawings is a multi-chip memory array discussed, except in that a means for providing sector erase capability is needed on page 3, lines 6-15.

In the office action, references were made to the paragraphs of the published application. For convenience, the above references correspond to paragraphs 0006, 0008 and 0009. It must be noted that the office action relies upon paragraphs 0008 and 0011 as showing that the AAPA includes multiple chips. As discussed above, paragraph 0008 specifically refers to FIG. 2 as being a single chip, and paragraph 0011 refers to a multi-sector erase operation of the single chip of FIG. 2. A single chip may have multiple sectors, but there is nothing in the AAPA that addresses multi-sector erase operations across multiple chips.

The office action also states that, "It would have been obvious to one of ordinary skill of the art at the time the invention was made to use the circuitry and signals described by Fling to connect to a plurality of memory chips, as it is obvious that if you can use the

circuitry to connect to one chip, you can connect to a plurality of chips." However, this is not true.

In order to connect to multiple chips, one must provide a means for determining which chip is currently active. There is no discussion of such a designation in either the AAPA, nor in Fling, as both are directed to single chips.

Claims 1, 7 and 13 have been amended to more clearly state that the chip information signal identifies a chip from the plurality of chips. This is not shown, taught nor suggested by neither the AAPA, nor Fling. It would not have been obvious over these references as there is neither need nor motivation in either reference to designate one from multiple chips as both references are single chips only.

It is therefore submitted that claims 1, 7 and 13 are patentably distinguishable over the prior art and allowance of these claims is requested.

Claims 2-3 and 5 depend from claim 1, claims 8-9 and 11 depend from claim 7, and claims 14-15 and 17 depend from claim 13. These claims inherently contain all of the limitations of their respective base claim. As discussed above, the prior art does not teach, show nor suggest all of the limitations of the base claim, much less the further embodiments of the dependent claims. It is therefore submitted that these claims are patentably distinguishable over the prior art and allowance of these claims is requested.

Claims 4, 10 and 16 were rejected under 35 U.S.C. 103(a) over the AAPA in view of Fling and further in view of Peri, U.S. Patent No. 6,904,400.

The AAPA and Fling do not teach all of the limitations of the base claim. Peri is also directed to a single chip system. Therefore, even if Peri did teach information in a hard-coded option, Peri does not teach a chip selection signal that designates one chip from a plurality of memory chips as a hard-coded option. It is therefore submitted that claims 4, 10 and 6 are patentably distinguishable over the prior art and allowance of these claims is requested.

Claims 6, 12 and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Fling and further in view of Fukumoto.

The AAPA and Fling do not teach all of the limitations of the base claim. Fukumoto is also directed to a single chip system. Therefore, even if Fukumoto did teach a counter corresponding to a most significant address bit, Fukumoto does not teach chip information that designates one chip from a plurality of memory chips as a most significant bit. It is therefore submitted that claims 6, 12 and 18 are patentably distinguishable over the prior art and allowance of these claims is requested.

With regard to claims 19-21, the same amendment clarifying that the chip information identifies one chip from a plurality of chips has been made to claim 19. Therefore, for the reasons discussed above, it is submitted that claims 19-21 are patentably distinguishable over the prior art and allowance of these claims is requested.

For the foregoing reasons, reconsideration and allowance of claims 1-21 of the application as amended is solicited. No new matter has been added by this amendment. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on January 31, 2006.

Li Mei Vermilya

Dong-Hyuk CHAE, et al.
SEMICONDUCTOR MEMORY SYSTEM AND METHOD FRO MULTI-SECTOR ERASE OPERATION
Attorney Docket No. 4591-390/Application No. 10/822,167

Annotated Sheet Showing Changes

Fig. 1

(PRIOR ART)

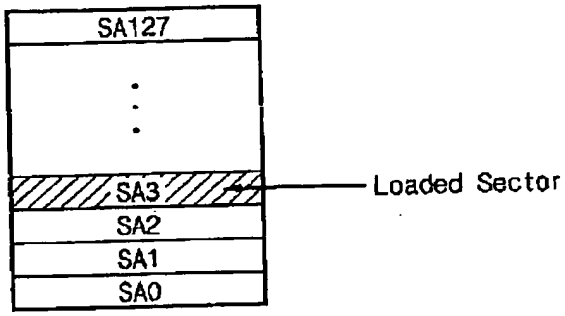


Fig. 2

(PRIOR ART)

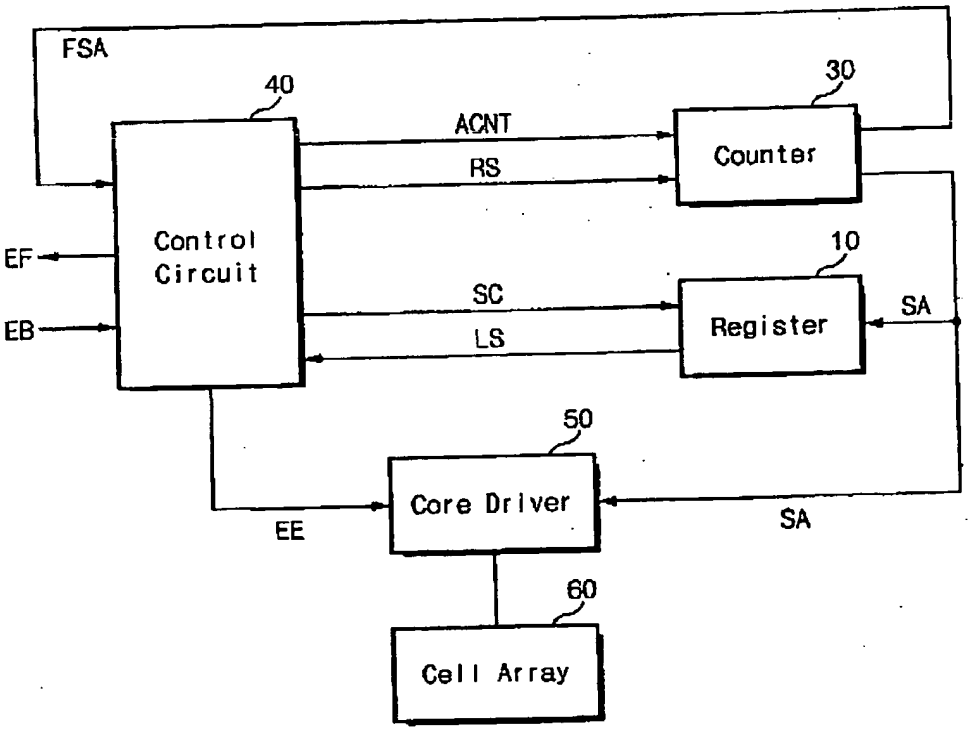


Fig. 3

(PRIOR ART)

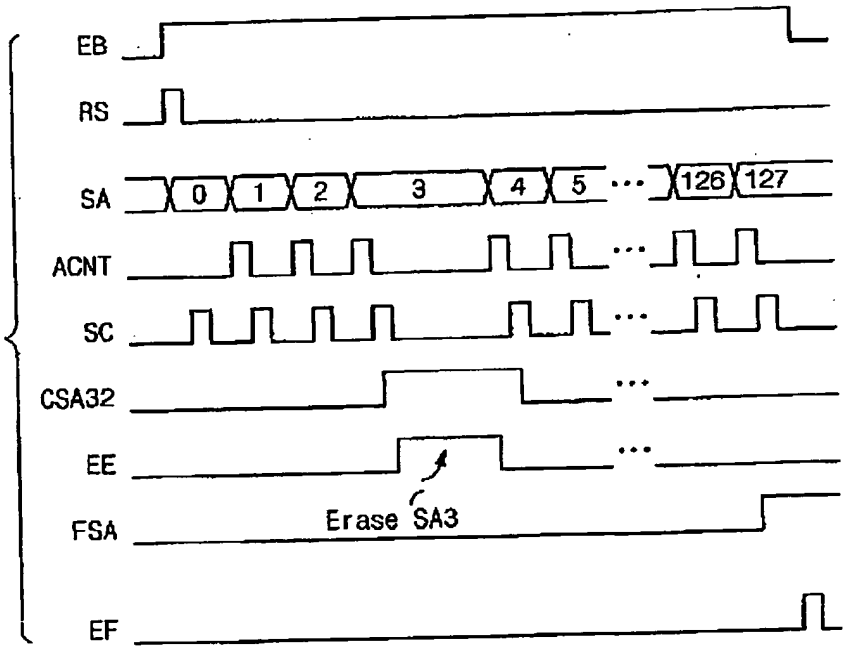


Fig. 4

(PRIOR ART)

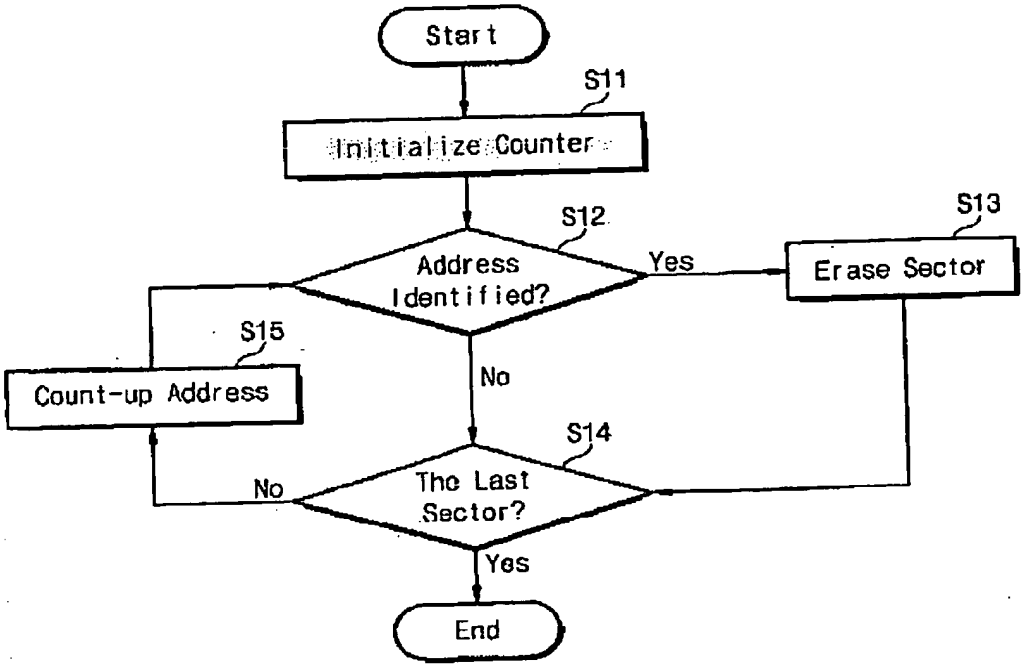
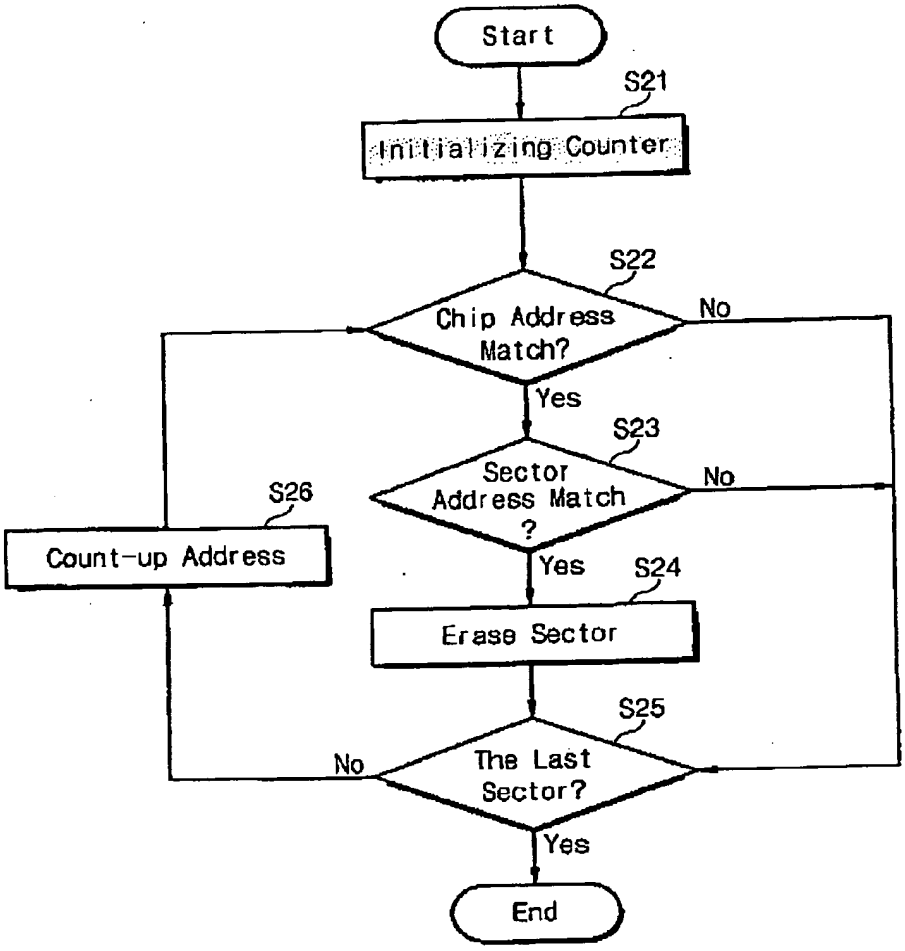


Fig. 11


Start
S21
Initializing Counter
S22
Chip Address Match?
No
Yes
S23
Sector Address Match ?
No
S26
Count-up Address
Yes
S24
Erase Sector
S25
No
The Last Sector?
Yes
End